In the Claims

1. (Currently Amended) An integrated circuit, comprising:

a semiconductor substrate having a major body portion;

a conductive layer having a predefined boundary and located on a first surface of the major body portion[;] , said conductive layer formed with individual fingers;

an insulating layer positioned over the conductive layer;

an integrated inductor located on the insulating layer over the conductive layer;

an inductor having a current path that crosses the short dimension of said finger; and

an amplifier connected between the integrated inductor and the conductive layer.

2. (Original) The integrated circuit according to claim 1 wherein the integrated inductor has a predefined length with a center position and an input to that amplifier is connected to the center position.

3. (Original) The integrated circuit according to claim 1 wherein the integrated inductor has a predefined inductance with a center position dividing the inductance and an input to that amplifier is connected to the center position.

PAGE 3/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

4. (Original) The integrated circuit according to claim 1 further comprising a second amplifier and wherein the integrated inductor has a predefined length comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

5. (Original) The integrated circuit according to claim 4 wherein the first, second and third portions all are of equal length.

6. (Original) The integrated circuit according to claim 1 further comprising a second amplifier and wherein the integrated inductor has a predefined inductance comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

PAGE 4/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

7. (Original) The integrated circuit according to claim 6 wherein the first, second and third portions are all of equal inductance.

8. (Original) The integrated circuit of claim 1 wherein the amplifier has a voltage gain of one or less.

9. (Currently Amended) An integrated circuit [of] comprising:

a semiconductor substrate having a major body portion;

a conductive layer having a predefined boundary and fingers and located on a first surface of the major body portion;

an insulating layer positioned over the conductive layer;

an integrated inductor located on the insulating layer over the conductive layer;

wherein at least some portion of a current path of an inductor being approximately perpendicular to direction of long portion of said fingers; and

wherein at least one portion of said conductive layer is biased to an ac potential, which is representative of the ac voltage at some point on said inductor.

PAGE 5/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

10. (Currently Amended) The integrated circuit according to claim 9 and including a first amplifier wherein the integrated inductor has a predefined length with a center position and an input to said [that] amplifier that is connected to the center position.

11. (Currently Amended) The integrated circuit according to claim 9 and including the amplifier wherein the integrated inductor has a predefined inductance with a center position dividing the inductance and an input to [that] an amplifier that is connected to the center position.

12. (Currently Amended) The integrated circuit according to claim 9 further comprising [a] the first and second amplifier and wherein the integrated inductor has a predefined length comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

13. (Original) The integrated circuit according to claim 12 wherein the first, second and third portions all are of equal length.

PAGE 6/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

14. (Currently Amended) The integrated circuit according to claim 9 further comprising [a] the first and second amplifier and wherein the integrated inductor has a predefined inductance comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

15. (Original) The integrated circuit according to claim 14 wherein the first, second and third portions are all of equal inductance.

16. (Currently Amended) The integrated circuit of claim 9 wherein the amplifier has a voltage gain of [one] OdB or less.

17. (Currently Amended) A method for increasing the self-resonant frequency of [on] an integrated inductor by:

forming a conductive layer beneath the inductor;

said conductive layer having a plurality of individual segments thereof, said plurality of segments underlying said inductor;

PAGE 7/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

forming an insulating layer between the conductive layer and the inductor; and

connecting an amplifier between the integrated inductor and the conductive layer.

18. (Original) The method according to claim 17 wherein the integrated inductor has a predefined length with a center position and an input to that amplifier is connected to the center position.

19. (Original) The method according to claim 17 wherein the integrated inductor has a predefined inductance with a center position dividing the inductance and an input to that amplifier is connected to the center position.

20. (Original) The method according to claim 17 further comprising a second amplifier and wherein the integrated inductor has a predefined length comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

PAGE 8/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

21.(Original) The method according to claim 20 wherein the first, second and third portions all are of equal length.

22. (Original) The method according to claim 17 further comprising a second amplifier and wherein the integrated inductor has a predefined inductance comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

23.(Original) The method according to claim 22 wherein the first, second and third portions are all of equal inductance.

24.(Original) The method of claim 17 wherein the amplifier has a voltage gain of one or less.

25. (Currently Amended) A circuit that includes an integrated inductor with its self-resonant frequency increased by:

PAGE 9/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

forming a conductive layer beneath the inductor;

said conductive layer being comprised of a number of individual fingers;

forming an insulating layer between the conductive layer and the inductor;

connecting an amplifier between the integrated inductor and the conductive layer.

26.(Original) A circuit according to claim 25 wherein the integrated inductor has a predefined length with a center position and an input to that amplifier is connected to the center position.

27.(Original) A circuit according to claim 25 wherein the integrated inductor has a predefined inductance with a center position dividing the inductance and an input to that amplifier is connected to the center position.

28.(Original) A circuit according to claim 25 further comprising a second amplifier and wherein the integrated inductor has a predefined length comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

PAGE 10/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04

29. (Original) The integrated circuit according to claim 28 wherein the first, second and third portions all are of equal length.

30. (Original) The integrated circuit according to claim 25 further comprising [a] the second amplifier and wherein the integrated inductor has a predefined inductance comprising a first portion, a second portion and a third portion with the second portion being electrically connected to the first portion at a first connection and the input to the amplifier being connected to the first connection and the third portion being electrically connected to the second portion at a second connection and an input to the second amplifier being connected to the second connection.

31.(Original) The integrated circuit according to claim 30 wherein the first, second and third portions are all of equal inductance.

32.(Currently Amended) The integrated circuit of claim 25 wherein the amplifier has a voltage gain of [one] QdB or less.

PAGE 11/14 * RCVD AT 4/6/2005 3:22:58 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/26 * DNIS:2738300 * CSID:9728667787 * DURATION (mm-ss):05-04